Crack and Damage Evaluation in low-k Interconnect Structures under Chip Package Interaction Aspects

J. Auersperg[1,2], D. Vogel[1], M.U. Lehr[3], M. Grillberger[3] and B. Michel[1]

[1] Fraunhofer IZM, Berlin and Fraunhofer ENAS, Chemnitz, Germany
[2] AMIC GmbH, Berlin, Germany
[3] AMD Fab36 LLC & Co. KG, Dresden, Germany

ABSTRACT. *Miniaturization and increasing functional integration as the electronic industry drives force the development of feature sizes down to the nanometer range. Moreover, harsh environmental conditions and new porous or nano-particle filled materials introduced on both chip and package level - low-k and ultra low-k materials in Back-end of line (BEoL) layers of advanced CMOS technologies, in particular - cause new challenges for reliability analysis and prediction. The authors show a combined numerical/experimental approach and results towards optimized fracture and fatigue resistance of those structures under chip package interaction aspects by making use of integral bulk and interface fracture concepts, VCCT and cohesive zone models in multi-scale and multi-failure modeling approaches with several kinds of failure/fatigue phenomena. Probable crack paths and interactions between material damaging, ratcheting and interface fracture will be discussed. As important preconditions for high-quality simulations, nano-indentation AFM, FIB and EBSD provide the desired properties, while FIB-based trench techniques using deformation analyses by grayscale correlation and numerical simulations provide the intrinsic stresses especially of thin films in BEoL layers.*

INTRODUCTION

Two major developments in electronics – miniaturization down to the nanometer range and introduction of new high-tech, nano-particle filled or nano-porous materials demand for innovative simulation techniques. An evident example is approaching by the latest technology developments for Back-end of line (BEoL) layers of advanced Cu/Low-k 90, 45…22 nanometer CMOS technologies. Under those conditions it is the big challenge for packaging to bridge the wide gap between chip (nm and µm range) and application (mm and cm range).

While the thermo-mechanical reliability is dependent on the layer/vias design and the materials used, it is additionally highly dependent on the interaction between the chip (incl. the BEoL layers) and the type, design, chosen materials, and manufacturing technology of the package – the so called chip package interaction (CPI) – see [1-2]. So, the wide range of structural dimensions – the nanometer range for the transistor and tiny

BEoL-structures and centimeter range for the overall design space of a device is one important challenge for FEA-simulations. Staying with “conventional” Finite Element Analysis implies global-local modeling (known as submodeling approach), multiple substructures (or superelements) as well as fracture and damage mechanics utilizing also cohesive zone models, visco-elasticity, plasticity (ratcheting under cyclic loading conditions) and creep of homogeneously constitutive behaving materials.

Assets and drawbacks of utilizing substructures and submodeling techniques are:

- Substructures as realized in FE-codes do not reflect nonlinearities - constitutive behavior of materials, contacts, CZM (cohesive zone method) etc.
- The evaluation of local deformation, strain and stress fields in substructures is possible but, there is no way to calculate fracture parameters (energy release rate ERR, J-integrals or stress intensity factors SIF).
- Making use of substructures is often coupled with a lot of fancy work and therefore fault-prone.
- It is necessary to pay attention to stiffening effects at the substructure-global model boundary or interlocking of substructures among themselves.

Otherwise:

- The submodeling approach has the advantage that it may contain nonlinearities, user written elements and materials and allows calculating fracture parameters etc. but, the results depend on the displacements at the boundary of the submodel taken from global model simulation results. If the global model is not precise enough, this can cause misleading results:

A BEoL-stack of a packaged microprocessor assembly (Lid removed -Fig. 1) was taken to make use of a substructures (forwards simulation of a global model with initial crack included) and submodeling technique (subsequent simulation for cracking/delamination risk evaluation) - see Fig. 1. Fig. 2 presents the submodel when deformed, with an initial crack in a bimaterial interface starting from underneath the chip corner with varying lengths.

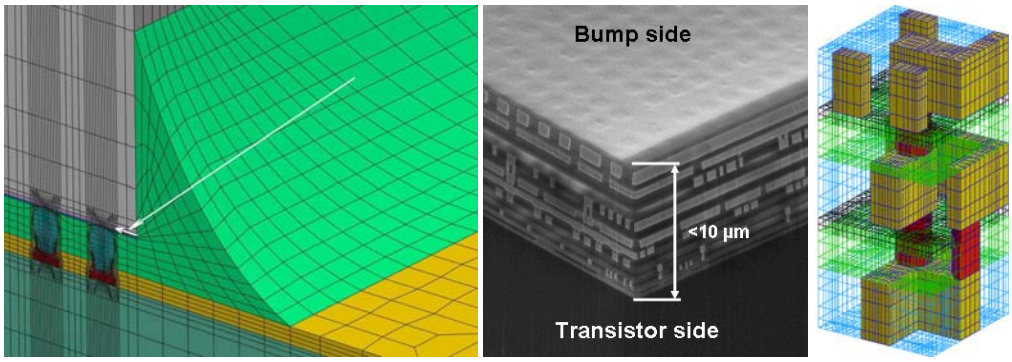

Figure 1. FC package without lid of a microprocessor with an initial crack in the BEoL-stack (left), BEoL stack (middle) and a 3D substructure detail (right)

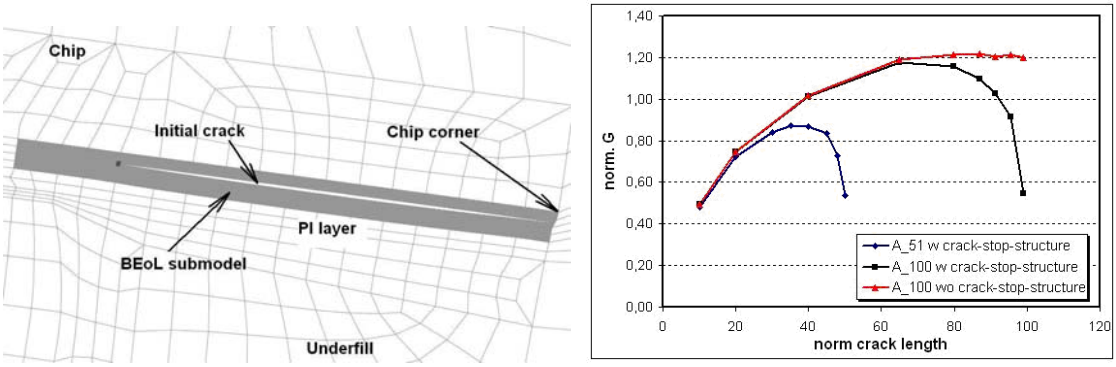

Figure 2. Submodel of the BEoL stack in a FC-assembly and normalized ERR vs. crack length for chip edge to crack stop structure distances 51 and 100

As to extract from Fig. 2, the crack driving force at the crack tip vs. the initial crack length under CPI increases up to a maximum and reduces close to the crack stop structure – assuming the crack stop structure is intact. The maximum achieved ERR depends on the chip edge to crack stop structure distance. This corresponds to the results in [2]. With no crack stop structure there is a saturation of the ERR.

So as to investigate the delamination risk of several material interfaces edge cracks of the BEoL stack various models with assumed initial crack were investigated - Fig. 3.

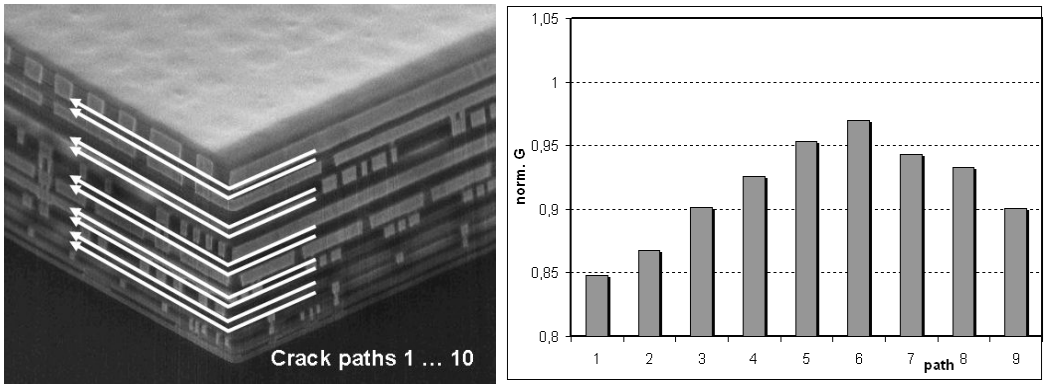

Figure 3. Assumed crack paths in BEoL structure and normalized ERR at the crack tip of several delamination paths

Initial bimaterial interface edge cracks along paths in the middle of the BEoL stack are the most critical ones – see Fig. 3. Going that way, sensitivity investigations due to the material selection, manufacturing processes, design parameters in the BEoL stack and of the whole package give information for further developments. On the other hand, cracks do not always propagate along material interfaces. As illustrated in Fig. 4, cracks propagate through ULK layers of BeoL stacks – bulk material crack popagation – after branching off from pure interface delamination. The phase angle of energy release rate $\Psi(G)$ shows clearly the mode II dominance under chip package interaction. Addition-

aly, damage propagation ahead of crack tips is also an important mechanism such as copper ratcheting too.

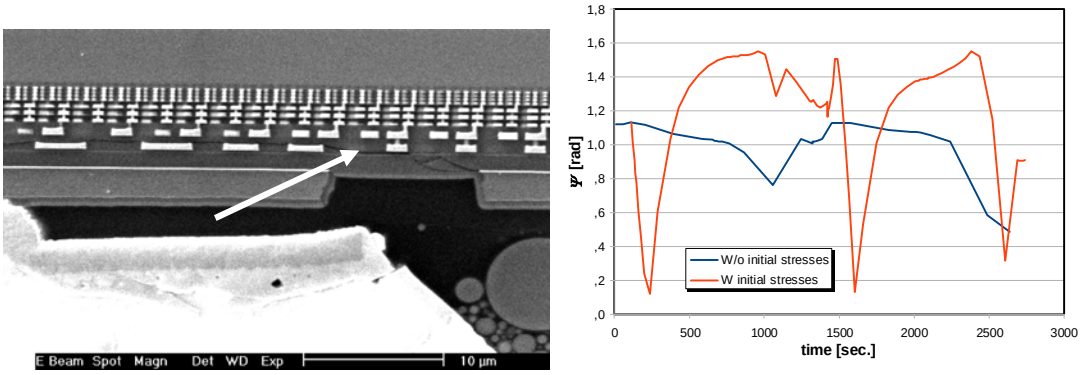

Figure 4. Crack propagating across a BeoL structures (left) and phase angle of ERR vs. time during assembly and thermal cycling with respect to initial stresses (right)

MULTI-SCALE MODELING – STRUCTURAL DEMANDS

Other challenges arise for instance from the close neighborhood of structural dimensions in design and morphology of newly developed materials in BEoL layers of advanced Cu/Low-k 90, 45…22 nanometer CMOS technologies. For example, porous SiCOH used as new materials in low-k BEoL stacks are increasingly porous and interconnect materials or new functional layers come up as nano-particle filled high-tech compounds. Therefore, it is to be checked whether they can still be handled as homogeneous materials, anymore. To identify the constitutive behavior of those materials and the appropriate material properties is generally difficult, requires expensive techniques (SEM, AFM, AFAM, FIB, Raman spectrometry etc.) and preparations. Frequently, they can only be estimated with the help of additional assumptions – linearity, constant Poisson's ratio, stiffness of substrates or fastenings etc.

These difficulties and the urgent request for more knowledge about the physics determining the material behavior is the driving force for atomistic level simulations and molecular modeling. So, atomistic level simulations start to help explaining the physics of deformation and damage incl. size effects in the closest area of crack tips in nano systems [3-4], in MEMS devices [5] or underneath a nano-indenter [6], and support at the same time to close the gap to conventional FE-techniques with the help of different hybrid FE–MD–QM simulation algorithms [7]. Molecular dynamics (MD) techniques increase in popularity for polymeric materials, carbon nanotubes, -rings, -connectors etc. [8], to simulate and understand the moisture diffusion [9], the mechanical behavior and properties of certain bi-material interfaces [10] and to determine material properties [11].

Two major ways seem to satisfy the need for characterizing the underlying physics best and to close the gap between MD and FEM:

Direct incorporation of homogenized MD-models:

- Modeling and simulation of the molecular structure,
- Homogenization in a unit cell,
- Use it inside a macro-model.
- Such approaches could also base on FEM- or semi-analytical representations of the micro-structure – the field of meso-mechanics.

Extraction of mechanical properties for use in FEM:

- Modeling of the molecular structure,
- Simulations towards extraction of key-properties, (Young's modulus, CTE, diffusion coefficients – see Figure 5)
- Use these properties in a macro-model, a FE-model for instance – see [12].

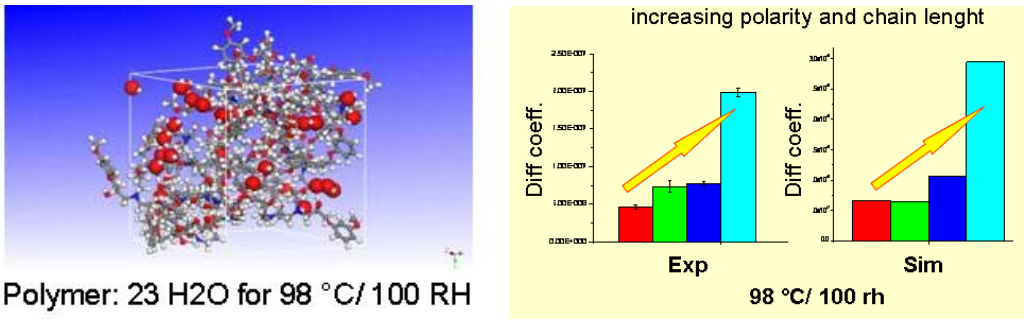

Figure 5. MD-simulation to extract moisture diffusion coefficients [12]

Because of the wide gap between MD and FEM and also because of the huge amount of computational resources necessary for appropriate MD simulations, the second way is preferred at the moment.

MULTIPLE FAILURE EVALUATION

Miniaturization, new materials and harsh environmental conditions cause new challenges for reliability analysis and prediction, i.e. the development of multiple failure criteria for combined loadings like residual stresses generated by several steps of the manufacturing process, various kinds of inhomogeneity, moisture diffusion and the well known thermal expansion mismatch problem. These circumstances, which can cause different failure modes like interface delamination, chip or encapsulation cracking, pop corning and/or fatigue of interconnects, have to be treated on a new qualitative level. Traditionally applied methodologies base on classical strength evaluations or/and life time estimations of solder interconnects by means of modified Coffin-Manson approaches, which rarely address multiple failure modes. Second, especially under cyclic loading conditions, fatigue of solder materials, fatigue crack propagation in polymers or at bimaterial interfaces and ratcheting of kinematic hardening metals take effect simultaneously. Therefore, approaches to evaluate such risks and damage propagation rates

have to provide qualitatively comparable results which speak the same language in order to use it for design optimizations.

It is to be noted that some of the accepted different risk and fatigue evaluating approaches are restricted to LEFM (SIF, mode separation for VCCT – see [13]), some have to be checked for path independence of the results (J- or M-integrals [16]) and some seem less applicable for unloading situations (J-integral, VCCT [14-15], ARE [20] etc.). While CZM [17-18] and XFEM [19] have the potential of incorporating micromechanical conditions and processes with some difficulties - mesh dependence, time integration instability and the huge number of model-parameters that have to be measured prior to the simulations. However, in sensitivity analysis and especially in optimization studies the overload preventing parameters can act as boundary conditions, nonlinearly restricting the allowable parameter window – see [21]. All fatigue evaluating approaches have to provide a consistent kind of measure in order to build a common objective function for multi objective optimizations. In as much, $\Delta a/\Delta N$ as provided by most of the approaches discussed above seems to constitute a good basis for that universal failure criterion.

MATERIAL PROPERTIES AND INITIAL STRESS STATE DETERMINATION

Complementary to the simulation side of reliability estimations, serious issues are connected with the collection of appropriate material properties in the miniaturized range addressed – Young's modulus, initial yield stress, hardening, in particular. In addition, residual stresses in the back-end layer stack caused by the different manufacturing processes have an essential impact on damage behavior, because they superpose functional and environmental loads [22]. Their determination with a spatial resolution necessarily for typical BEoL structure sizes is a critical issue. A determination of residual stresses by means of finite element simulations is problematic due to the large amount of process steps to be considered. Well established measurement methods either do not exhibit the necessary spatial resolution or show other limitations.

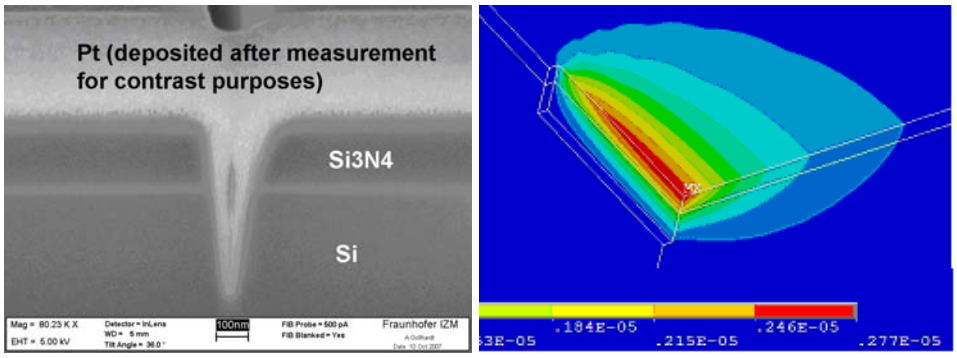

Figure 6. Trenches milled by focused ion beam equipment cause measurable local stress relief (left), measured deformations nearby trenches are compared with finite element-simulations in order to extract residual stresses

That's why new stress measurement methods with high spatial resolution are developed by the authors. Among them are nano-scale stress relief techniques (fibDAC), nanoRaman and electron backscattering (EBSD) based approaches. E.g., the fibDAC makes use of tiny trenches placed with a focused ion beam equipment at the position of stress measurement. Digital image correlation algorithms applied to SEM micrographs captured before and after ion milling allow to conclude on stresses released. Residual stresses can be computed with the help of appropriate FEA models [23-26] – see Fig. 6.

CONCLUSIONS

Feature sizes at the nanometer range and the introduction of new high-tech, nanoparticle filled or nano-porous materials cause novel challenges for reliability analysis and prediction of microelectronics assemblies, i.e. the development of multiple failure criteria for combined loadings including residual stresses, interface delamination, cracking and fatigue of interconnects simultaneously. The authors face up to multiscale modeling approaches, damage and fracture mechanics approaches on the basis of continuum mechanics and molecular dynamics approaches. Reliability predictions of miniaturized multi-material systems frequently require considering not only the variety of loadings and combined multiple failure criteria, but also intrinsic stress situations from previous technological steps. A new analysis technique based on stress release by FIB milling and high-resolution displacement measurement has been proposed.

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