"FRACTURE ELECTRONICS" - APPLICATION OF FRACTURE MECHANICS TO MICROELECTRONIC SYSTEMS AND CHIP PACKAGES

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ABSTRACT

The authors address the issue of cracks in thermo-mechanically stressed microelectronic assemblies. Special attention will be given to chips embedded in electronic packages. Cracks in microsystems excert an important influence on the reliability of electronic products. Some problems of chip card fracture will be dealt with using finite element analysis combined with in-situ-experiments by means of microDAC method, acoustic microscopy, laser scanning microscopy and micro moiré method.

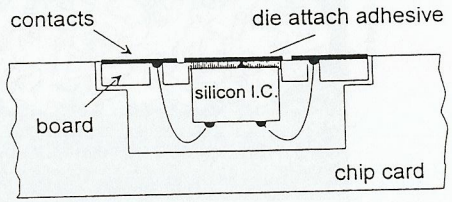
KEYWORDS

Fracture in electronics, microdeformation analysis, cracks in chips, cracks in microsystems, cracks in smart cards.

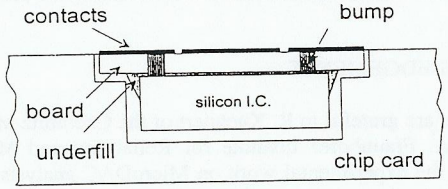
INTRODUCTION

Packaging of electronic circuits has become an important field of research activities in the last years. Many new packaging technologies ranging from surface mount technology (SMT), multichip modules (MCM), chip size packaging (CSP) to hybrid packaging have emerged. With growing miniaturization of the products the "local" material properties and local temperature gradients excert a greater influence on the reliability of microsystems than in any macroscopic components. Various kinds of inhomogeneities, localized internal stresses and the phenomena related to the so-called "thermal misfit" have to be taken into account. Crack and fracture phenomena in microsystems have to be taken into account more often. The expression "Fracture Electronics" has been used recently to characterize the growing activities in the field of fracture analysis applied to microelectronics and microsystem technologies (e.g. micromachining). Most of the microcomponents will become smaller and smaller

whereas the total chip size will be increased in the near future. Therefore, the problems of chip fracture and package fracture will become more and more important for quality assurance in microtechnology. Local deformation and crack phenomena of chips and in chip packages have to be studied in more detail. Simulation methods which are directly combined with modern experimental techniques (e.g. laser technique, acoustic microscopy) will be more often used for reliability estimations of microcomponents and microsystems. The paper presents numerical simulation and experimental investigations on modules embedded in card pockets consisting of silicon, FR-4 board substrate, and of a thin metal layer as contact plate under different test conditions. Fig. 1 shows two packaging technologies which are widely used to produce telephone cards and other chip cards (smart cards). These are wire bond and flip chip technologies, respectively.



(a)



(b)

Fig. 1: Chip card design based on wire bond (a) and flip chip interconnection technologies (b), respectively

Figure 2 shows a typical micropackage of a silicon chip surmounted on a so-called leadframe. The encapsulation usually is performed through a special molding compound (plastic package). The assembly consists of very different materials. Thermal and mechanical loading leads to misfit-problems and subsequent cracking processes.

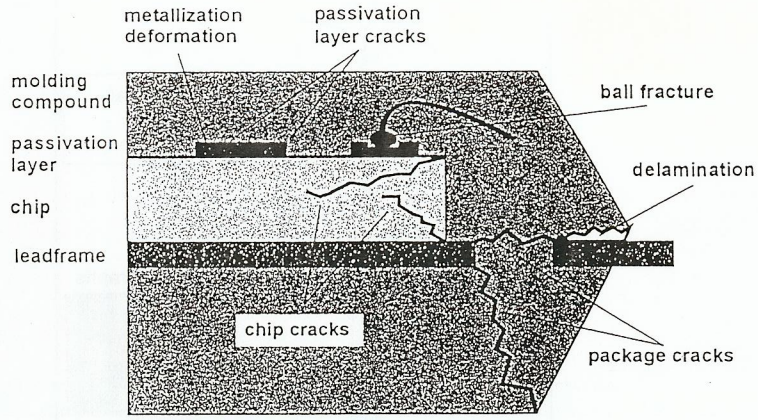


Fig. 2: Characteristic failure modes and cracking patterns of a chip package

MICRODEFORMATION ANALYSIS AROUND CRACKS NEAR MICRO SOLDER BUMPS

There is a great interest in advanced techniques to study the microscopic deformation as well as to verify numerical simulations. Field measuring techniques using laser metrology have been widely used also in various branches of microengineering, e.g. microsystem technologies. The electron microscope has also been a good means for a long time to study microdeformation. The so-called Micro Moiré method applies a special grid preparation to study the changes in moiré interference patterns during in-situ-deformation of micro specimens in SEM. Figure 3 shows the principle of crack deformation analysis using Micro Moiré method in SEM.

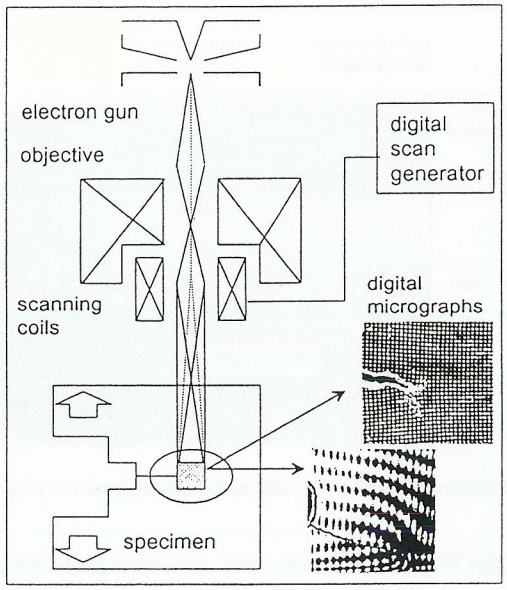


Fig. 3: Principle of Micro Moiré analysis of a near crack deformation field using a scanning electron microscope

The Micro Moiré technique works interferometrically and is a high precision measuring technique for the study of deformation field around micro cracks. As this method requires a prepared surface grid in the region to be analyzed the costs are very high. A low-cost method which does not need a reference grid is the so-called MicroDAC method (Micro Deformation Analysis by means of Correlation Methods). It uses the grey level distribution of the digital SEM micrographs that represent the registered signal intensity of an object structure at a given moment. The displacements of any point during each load step is determined by correlation method (real displacements are shown to be characterized by a maximum of the image correlation function). The method enables the measurement of plane displacement components without any additional preparation in regions of about $100 \times 100\ \mu m^2$ (see Fig. 4 for an example).
The paper will give more-detailed information about the crack behaviour within the defected regions of micro solder bumps and other components of microsystems. Special attention will be given to the fracture behaviour of chip card components, where very different materials are combined within the interconnection regions (silicon chip, polymeric adhesive, metallic solder material, the board which often consists of FR-4 composite or ceramics). The effect of creep crack growth was investigated too. The thermofatigue behaviour of cracks arising in the solder region will be discussed. Reliability estimations for the components follow which are in a very good agreement with the real failure behaviour of the microelectronic components. The procedure has been successfully applied to evaluate some microsensor packages for automotive applications (airbag sensors), a microwave feed through of a radar sensor, and for packages of multichip modules used in telecommunication. The results obtained for the above-mentioned application by means of MicroDAC method and FEM were also

compared with results obtained from other experiments using mainly laser scanning microscopy and acoustic microscopy.

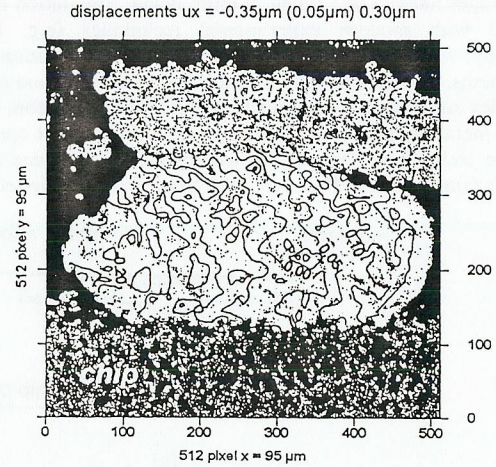


Fig. 4: Thermal deformation field of a microcrack at a solder bump on a microchip

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