Effect of Sidewall Morphology on the Fracture and Fatigue Properties of Polysilicon Structural Films

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Abstract

This study highlights the difference in the sidewall morphology of *n*+-type polysilicon films from two popular microelectromechanical systems (MEMS) processes and its effect on fracture and fatigue properties. Atomic force and transmission electron microscopy show that thick silicon oxides (20 ± 5 nm) are found in PolyMUMPs films, caused by galvanic corrosion from the presence of gold on the chip, whereas in SUMMiT films a much thinner (3.5 ± 1.0 nm) native oxide was observed. These thicker oxide layers, in combination with differences in sidewall roughness (14 ± 5 nm for PolyMUMPs and 10 ± 2 nm for SUMMiT), have a significant effect on the fracture and fatigue properties of polysilicon structures; this is shown by measuring fracture strength (3.8 ± 0.3 GPa for PolyMUMPs and 4.8 ± 0.2 GPa for SUMMiT) and stress-lifetime high-cyclic fatigue curves.

1. Introduction

Because of their large surface to volume ratio, the surfaces properties of structural thin films used in MEMS have a significant effect on fracture and fatigue properties. Consequently, it is imperative to fully characterize the surfaces of the materials and components used in MEMS designs in order to correctly predict device reliability. Since silicon is currently one of the main materials used in MEMS and many devices contain in-plane flexures [1], this study is focused on the influence of sidewall morphology and silicon oxide thicknesses on fracture strength and cyclic fatigue resistance in bending of micrometer-scale polycrystalline (polysilicon) structural films. For thin films, the thickness of the silicon oxide layer and the sidewall roughness can affect fracture behavior [2-5]. As the fracture toughness of silicon (K_c ~ 1 MPa√m [6]) is 15% higher than that of silicon oxide (K_c ~ 0.85 MPa√m [7]), a thick oxide layer on a micrometer-scale silicon film can be weakening. More importantly, unlike (macro-scale) silicon [8-11], silicon oxide is susceptible to environmentally-assisted subcritical cracking [12]. Such subcritical crack growth in SiO_2 occurs at stress intensities that are a factor of three or so lower than the fracture toughness, specifically above a threshold stress intensity factor of K_{TH} ~ 0.25 MPa√m [13]. This latter

phenomenon has been associated with observations that micrometer-scale structural films of silicon are susceptible to failure under high-cycle fatigue loading. Specifically, moisture-assisted subcritical cracking within a cyclic stress-assisted thickened oxide layer that becomes thick enough to accommodate critical crack sizes can result in catastrophic failure, a process that has been named "reaction-layer" fatigue [13-18].[1] These studies also revealed that the oxide thickness in post-release thin film silicon structures, rather than being only a few nanometers thick as is regularly assumed (*e.g.,* [21]), can sometimes be significantly larger. Scanning and transmission electron microscopy (respectively, SEM and TEM) is combined with atomic force microscopy (AFM) to characterize the polysilicon sidewall surface and silicon/silicon oxide interface, and to obtain sidewall surface roughness, silicon oxide thickness and in-plane grain size measurements. These measurements are correlated with the measured fracture and fatigue behavior.

2. Experimental methods

Fracture and fatigue and post-release sidewall surfaces from both the MEMSCAP PolyMUMPs and Sandia National Laboratories SUMMiT V n^+-type polysilicon processes were studied. The PolyMUMPs devices examined had been 49% HF released according to the release process prescribed in the process manual for 3 min [22]. The SUMMiT V films that were used for SEM and AFM imaging had a perflurordecyltrichlorosilane, $CF_3(CF_2)_7(CH_2)_2SiCl_3$ (PFTS) mono-layer coating deposited on them during the release procedure[2], whereas the films used for the oxide thickness measurements and all measurements of fracture strength and fatigue endurance did not. Further details of the process flows for the two polysilicon fabrication processes can be found in Refs. [22-24].

Fracture strength and fatigue experiments were performed using electrostatically-actuated resonator devices without mono-layer coatings, as described in Ref. [17]. The device consists of a ~300 μm sided triangularly shaped free-standing proof mass connected to an anchor on the substrate by a notched cantilever beam. The mass is electrostatically driven in-plane at resonance (~ 36-40 kHz) with fully reversed loading (ratio of minimum to maximum stress, R = -1) by an interdigited comb drive at one side of the device, whereas the comb structure on the other side of the proof mass is used to capacitively sense the displacement of the device

[1] It should be noted that the mechanisms associated with the fatigue of silicon thin films are still the subject of some debate. For a more in-depth discussion, the reader is referred to the following reviews and viewpoint papers in refs. [16,18-20].

[2] The coating was applied during the release procedure via the following steps in solution at room temperature: release etched (HF:HCL for 90 min), rinsed with deionized (DI) water, oxidized with H_2O_2, rinsed with DI water, transferred to isopropyl alcohol and then to iso-octane, transferred to 1 mM solution of the monolayer in iso-octane and held in solution for 2 hr, transferred to neat iso-octane, then to isopropyl alcohol and to DI water, before finally being removed from DI water and air dried on class 10 clean bench.

during operation. Using the measured (calibrated) displacement and finite-element calculations, the stress at the notch in the cantilever beam during the test can be calculated [17]. The fatigue experiments shown here were all conducted in ambient air at room temperature (25°C, 30-40% relative humidity). Corresponding fracture strength experiments were carried out by quickly following the resonance curve of the structures by rapidly increasing the driving frequency with a high applied driving voltage up to fracture. In order to mitigate any effect of the cyclic actuation and environmental decay of the structure, all fracture strength tests were operated at room temperature in a high vacuum (pressures $< 2.0 \times 10^{-7}$ mbar), which prevented the occurrence of any damage from environmentally-assisted subcritical cracking [17].

TEM and AFM samples were prepared using focused-ion beam (FIB) lift-out sample preparation techniques [25,26]. SEM imaging was carried out using a FEI Strata DB235 Dual Beam FIB at 5kV. TEM imaging was performed in both a 300 kV JEOL 3010 and Philips CM200-FEG operated at 200 keV. Energy-filtered transmission electron microscopy (EFTEM) allowed the creation of an elemental (in this case, oxygen) map of an area of interest. The AFM measurements were performed using an Asylum Research MFP-3D instrument in non-contact mode. The root mean square (*rms*) roughness of the sidewall surfaces was measured in sample areas of roughly 4 μm^2 and then averaged over a number of measurements (19 for PolyMUMPs and 12 for SUMMiT V).

3. Results

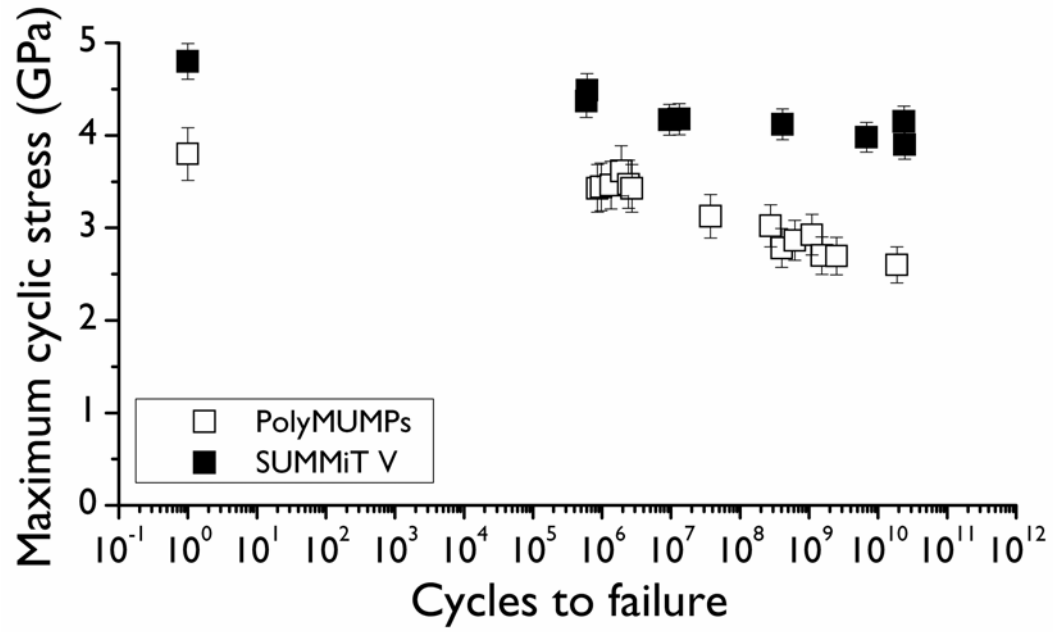

Fig. 1: Fracture strength (at 1 cycle to failure) and high-cycle fatigue lifetime ($> 10^5$ cycles to failure) in ambient air for PolyMUMPs and SUMMiT V fatigue resonator devices. After [27].

Results of fracture strength and fatigue lifetime tests for both PolyMUMPs and SUMMiT V devices are given in Fig. 1. The measured fracture strength of the SUMMiT V devices is some 26% higher than for the PolyMUMPs devices (respectively 3.8 ± 0.3 GPa and 4.8 ± 0.2 GPa). Similarly, the fatigue resistance of the SUMMiT V devices [17] is also higher than for the PolyMUMPs devices, the former not only having a higher single-cycle fracture strength, but also a more shallow slope in the high-cycle regime of the stress-lifetime plot (Fig. 1). This results in a 10^{10}-cycle fatigue endurance strength of the PolyMUMPs films that is ~35% lower than for the SUMMiT V films, *i.e.,* 2.6 ± 0.3 GPa, as compared to 4.0 ± 0.2 GPa. The locations of crack initiation were predominantly on the sidewall. This is indicated in Fig. 2 which shows typical fracture surfaces from fractured specimens of both the PolyMUMPs and SUMMiT V devices.

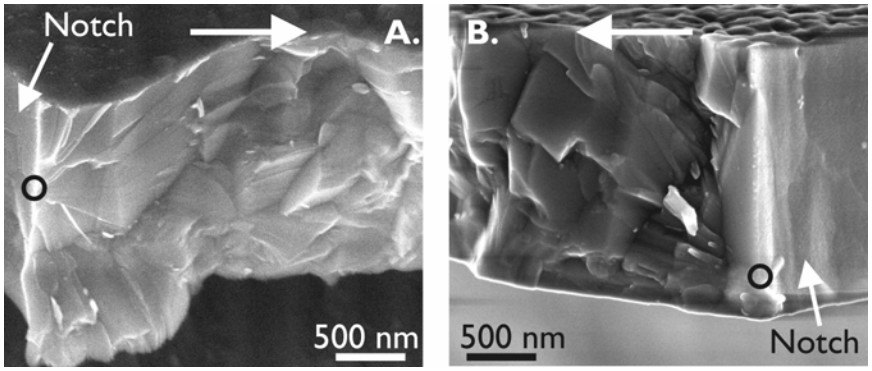

Fig. 2: Examples of fracture surfaces of fractured devices from the PolyMUMPs (A) and SUMMiT V (B) processes showing probable initiation points (marked with a circle) at the notch sidewall. The horizontal arrows indicate the direction of crack propagation. After [27].

The sidewall morphology of polysilicon films from both the PolyMUMPs and SUMMiT V process are shown in Figs. 3A and 4A. Grain sizes, quantified using the linear intercept method [28] from cross-sectional TEM views from the middle of the films (Figs. 3B, 4B), gave values for the PolyMUMPs films of 349 ± 23 nm, as compared to 435 ± 35 nm for the SUMMiT V films. AFM revealed an average *rms* roughness of the sidewalls of the PolyMUMPs devices to be 14 ± 5 nm, as compared to 10 ± 2 nm for the SUMMiT V films.

The morphologies of the oxide layer and the silicon/silicon oxide interface in the sidewalls of the PolyMUMPs and SUMMiT V polysilicon films are shown respectively in Figs. 3C and 4C. The exact thickness of the oxide film cannot be simply deduced from bright field TEM images, because of the presence of 'milling debris' which like the oxide layer has an amorphous structure. However, the EFTEM images (Figs. 3C, 4C) do clearly show the silicon oxide. The silicon oxide layers in the SUMMiT V films (Fig. 4C) were 3.5 ± 1.0 nm in thickness. In contrast, the oxide layers on the PolyMUMPs films (Fig 3C) were three to five times thicker (20 ± 5 nm in thickness), with a much rougher Si/SiO_2 interface.

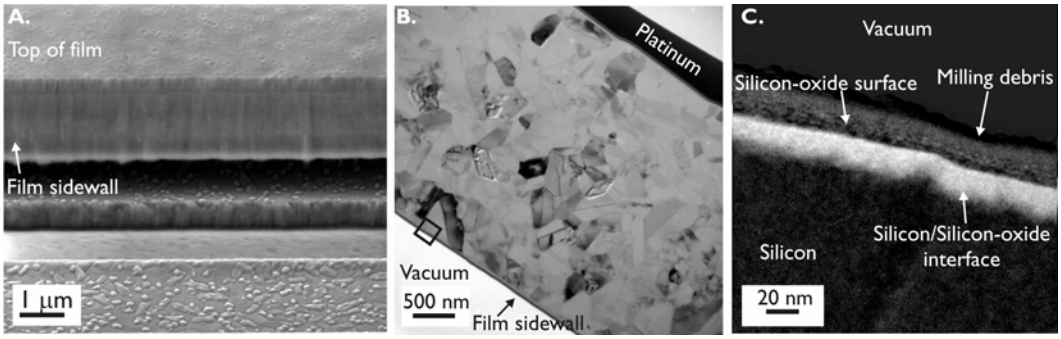

Fig. 3: (A) PolyMUMPs SEM sidewall surface as seen from a 52 degree angle of incidence and (B) TEM cross-section as seen from the top of the film, along the axis of the in-plane grains. The orientation of the images in (C) is marked with a square. (C) EFTEM oxygen map showing silicon-oxide (thickness: 15 – 25 nm). The edge of the sample is marked by the vacuum. After [27].

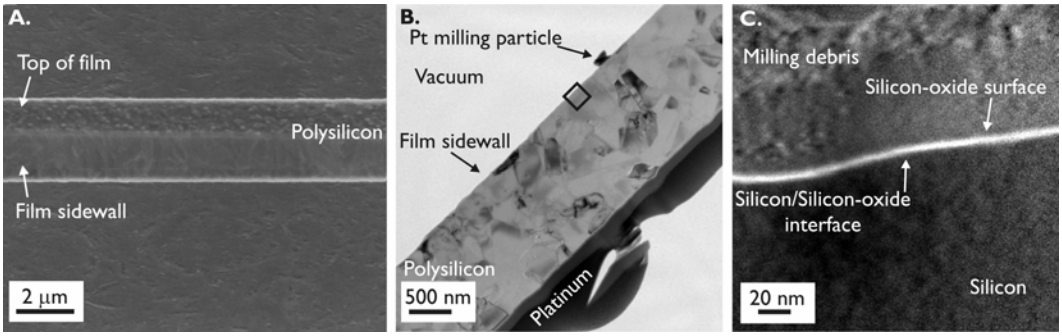

Fig. 4: (A) SUMMiT V SEM sidewall surface as seen from a 52 degrees angle of incidence and (B) TEM cross-section as seen from the top of the film, along the axis of the in-plane grains. The orientation of the images in (C) is marked with a square. (C) EFTEM oxygen map showing silicon-oxide (thickness: 2.5 - 4.5 nm). After [27].

4. Discussion

The measured difference in sidewall surface oxide thickness and Si/SiO_2 interface morphology between both fabrication processes (Figs. 3C, 4C) can be attributed to the different mechanisms that lead to the formation of the oxide. In the case of the SUMMiT V structures, a post-release native oxide is known to grow and then self-passivate after several nanometers of growth [29]. Thicker oxide layers on the PolyMUMPs films are known to be associated with a galvanic corrosion process during the HF release step [30,31]. Similarly, other differences in morphology can be explained by differences in processing conditions. Although both processes use low-pressure chemical-vapor deposited (LPCVD) polysilicon, followed by subsequent annealing steps, and are patterned using reactive-ion etching (RIE), the SUMMiT V polysilicon is phosphorous-doped during film deposition, while for the PolyMUMPs process the phosphorous is diffused into the polysilicon from sacrificial phosphosilicate glass (PSG) layers [22,32]. This difference in doping method can have an important effect on the stress-state in the film and thus on the grain size [32]. The larger grain size of the SUMMiT V films can be contributed to the differences between doping methods; specifically, SUMMiT V films are subjected to more high-temperature processing

steps after deposition of the particular layers studied here. Because of longer annealing times, the grains have more time to grow to a lower energy configuration. This difference in grain size in turn affects the roughness of the sidewalls; grain boundaries etch more readily during patterning of the film, resulting in deeper grooves at grain boundaries [33], and larger grain size will result into a lower number of grain boundaries per unit sidewall length, therefore lowering the sidewall roughness. The larger grain size of the SUMMiT V devices is consistent with their lower measured sidewall surface roughness

We ascribe differences in the fracture and fatigue behavior of the two types of devices to the effect of the sidewall morphology; however, for this to be meaningful, it is important to verify that the failure origin of the specimens is actually on the sidewalls. The *rms* roughness of the top surface for the SUMMiT V films is in the order of 3.5 ± 2.1 [34], lower than the sidewall roughness, and for the PolyMUMPs films it is 13 ± 1 nm [35,36], similar to the sidewall roughness. Additionally, the top of the PolyMUMPs films have deeper and sharper grain boundary cusps than the sidewall [37,38]. This could result in a potentially important contribution of the morphology of the top of the films. However, since these tests are conducted in in-plane bending, the sidewall area is one of the regions on the device subjected to the highest stresses, and thus there is a larger probability of a pre-existing defect initiating a fracture there. In addition, the small top film surface area that is under high stress will be less constrained than most of the sidewall, leading to stress relaxation there. Moreover, river markings on the cleavage facets on the fracture surfaces close to the notch root all strongly imply fracture initiation at the sidewall (Fig. 2). Specifically, the fracture surfaces for the PolyMUMPs devices (Fig. 2A) show failure initiation at sidewalls or at the intersection of the sidewalls and the top/bottom of the film; corresponding fracture initiation in the SUMMiT V devices (Fig. 2B) occurred mostly at the sidewall.

In general, the measured difference in fracture strength between the PolyMUMPs and the SUMMiT V devices (Fig. 1) can be related to two morphological factors: the sidewall roughness and the oxide layer thickness. As discussed above, as silicon oxide has a lower fracture toughness than silicon (*i.e.*, ~0.85 *vs*. 1.0 MPa√m), this translates in micrometer-sized structural films to critical crack sizes (for catastrophic failure) that are typically up to tens of nanometers long [39]. Correspondingly, the presence of a ~20-nm thick oxide layer (instead of a ~3.5 nm native post-release oxide) can negatively affect the fracture resistance. More importantly, the higher sidewall roughness for PolyMUMPs (14 ± 5 nm versus 10 ± 2 nm for SUMMiT V) and the additional effect of the roughness at the top of the film contributes to its lower fracture strength, as this can be directly related to the presence of larger surface flaws in the material, and hence lower stresses to fracture the specimens. This marked dependence on the roughness (and hence on a higher preponderance of flaws in the device) is reflected by the fact that although the fracture strength of polysilicon changes with different film

microstructures, the fracture toughness of thin-film polysilicon is essentially totally independent of microstructure [40].

In addition to the observed roughness and oxide thickness effect on fracture strength, the effect of different oxide layer thicknesses is seen more clearly in high-cycle fatigue behavior of these two types of polysilicon specimens (Fig. 1) [17]. With a possibility of cyclic stress-assisted (moisture-induced) subcritical cracking occurring in the oxide layer, which is the mechanism for high-cycle fatigue of micrometer-scale silicon, the initial oxide layer thickness becomes a critical parameter; thicker initial oxides cause the devices to fail earlier because the oxide does not have to grow so much in order to reach the thickness needed to accommodate the critical crack sizes. Indeed, such a difference in fatigue resistance due to different silicon oxide layer thicknesses has indeed been observed (Fig. 1) [17]. For PolyMUMPs devices the fatigue resistance is significantly lower than for SUMMiT V; this is apparent from the observed steeper slopes in the stress-lifetime fatigue data for PolyMUMPs samples. This effect, in combination with the lower single-cycle fracture strength, results in a 10^{10}-cycle fatigue endurance strength of the PolyMUMPs films that is ~35% lower than for the SUMMiT V films, *i.e.,* 2.6 ± 0.3 GPa, as compared to 4.0 ± 0.2 GPa. These results are consistent with the fact that polysilicon from the SUMMiT V process has a thinner post-release oxide (~3.5 nm *vs*. ~20 nm for the PolyMUMPs).

5. Conclusions

Sidewalls of structures from two frequently used MEMS processes, PolyMUMPs and SUMMiT V, were characterized and related to the measured fracture strength and cyclic fatigue resistance. These measurements show that the post-release silicon oxides in MEMS processed devices can be much thicker than the few nanometers thick native oxide; moreover, the roughness of the silicon/silicon oxide interface is markedly influenced by the oxidation mechanism. Both factors can significantly affect damage-tolerant properties of the films. The specific conclusions from this study are:

1. Thick (20 ± 5 nm) silicon oxide layers, associated with galvanic corrosion during the HF release step due to the presence of gold on the chip, were found in the PolyMUMPs polysilicon films, in contrast to the thin (3.5 ± 1.0 nm) native oxide layers in the SUMMIT V films.
2. Together with the in-plane grain size, thicker oxide layers in the PolyMUMPs films were associated with increased surface roughness of the sidewalls and with increased roughness at the Si/SiO_2 interface. The PolyMUMPs films displayed a surface roughness of 14 ± 5 nm, as compared to 10 ± 2 nm for the SUMMiT V films.
3. Due to their five-fold thicker oxides, 40% rougher sidewalls and roughness of the top of the film, measured fracture strengths for the PolyMUMPs films were over 20% lower than for the SUMMiT V films, *i.e.,* 3.8 ± 0.3 GPa, as compared to 4.8 ± 0.2 GPa.

4. Similarly, the thicker oxides and lower fracture strengths of the PolyMUMPs films resulted in an increased susceptibility of these films to cyclic fatigue failure, which are believed to fail by environmentally-assisted subcritical cracking in a cyclic-stress assisted thickened silicon oxide. Specifically, the 10^{10}-cycle fatigue endurance strength of the PolyMUMPs films was ~35% lower than for the SUMMiT V films, *i.e.,* 2.6 ± 0.3 GPa, as compared to 4.0 ± 0.2 GPa.

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